ABSTRACT

[00112] Embodiments of the invention provide a programmable FSA building block, having a number of programmable registers and associated logic implemented therein, that provide the capability of contextually evaluating complex REs of arbitrary size against multiple data streams. Embodiments of the invention provide fully programmable hardware in which all of the states of an RE are instantiated and all of the states are fully connected. For one embodiment, the building blocks have a fixed number of states to facilitate implementation on a chip. For such an embodiment, an RE having an excessive number of states is implemented on two or more FSA building blocks and the FSA building blocks are then stitched together to effect evaluation of the RE. For one embodiment, two or more REs having a number of states less than the fixed number of states of a building block may be implemented with a single building block.